Application No.: 09/826,035 Docket No.: 21806-00123-US

REMARKS

Claims 1-21 are pending in the application. Favorable reconsideration is requested.

Withdrawal of the rejection of claims 1-20 as being anticipated under 35 U.S.C. § 102(e) by Devins et al. (U.S. Pat. No. 6,539,522) is requested. The present invention relates to a system to verify the interface of a core of a system on chip. In carrying out the invention, a mirror interface identical to the external internal interface on the core is created. A bus functional interface which models an internal bus and a processor model admits CPU cycles which emulate a processor. A control mechanism of the bus functional interface controls the flow of data through the external interface and applies test stimuli to the external interface. A memory is formed as part of the bus functional interface to receive any data transferred from the external interface.

An external, bi-directional general purpose register I/O connects the system on a chip (SOC) to the bus functional interface. Test cases running on the SOC can transfer control directives through the bus functional interface to configure the mirror interface for a given test being executed in the core of the system on a chip.

Independent claim 1 and new claim 21 set forth a combination of elements which are not disclosed in Devins et al. (U.S. Pat. No. 6,539,522). Specifically, in reviewing the Devins et al. patent, a system is disclosed for developing reusable software to verify system on chip designs. The system and method according to the Devins et al. reference provides for a hierarchy of software levels. Lower level software is used to provide interfacing between a test case generated by upper level software and the simulated hardware representing the system on a chip (SOC). Different levels of programming languages for testing a device permit a device to be tested at all levels of development without recreating the lower level software. Thus, by using the subject matter of the '522 patent it is possible to fully exercise a design of both individual cores, as they are developed, and cores which function concurrently when interconnected as a system without redesigning the lower level software.

In viewing the reference, it is not where there is any description of a mirror interface which is configured during test through a external bi-directional general purpose I/O, or which uses the bus functional interface to control data flow through the mirror interface and external interface of the system on chip (SOC).

While the foregoing reference clearly provides a bus functional module as part of the process for implementing a test operating system (TOS) so that the TOS executes externally to the simulator creating the SOC, it does not disclose any mirror interface which is created to have the identical input and output connections of the external interface. The bus functional modules described in col. 13 appear as a way to verify that cores can communicate in certain protocols. The external bi-directional general purpose I/O of claims 1 and 21 which configures the mirror interface from control directives received from the system on a chip (SOC) during a test case is not disclosed in the reference.

In this respect, claims 3 and 4, for example, are unique in that they require the directives to be transferred between the design and a bus functional model, as well as configuring the mirror interface. The remaining claims which are directed to using this structure to verify a test case therefore remain undisclosed.

In view of the foregoing favorable reconsideration is believed to be in order.

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Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 09-0456, under Order No. 21806-00123-US from which the undersigned is authorized to draw.

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Respectfully submitted,

By _____

George R. Pettit, Reg. No. 27,369
CONNOLLY BOVE LODGE & HUTZ LLP
1990 M Street, N.W., Suite 800
Washington, DC 20036-3425
(202) 331-7111
(202) 293-6229 (Fax)
Attorney for Applicant